Millimetre-Wave Circuit Simulation Challenges

EEsof Account Manager

15TH MAY 2019

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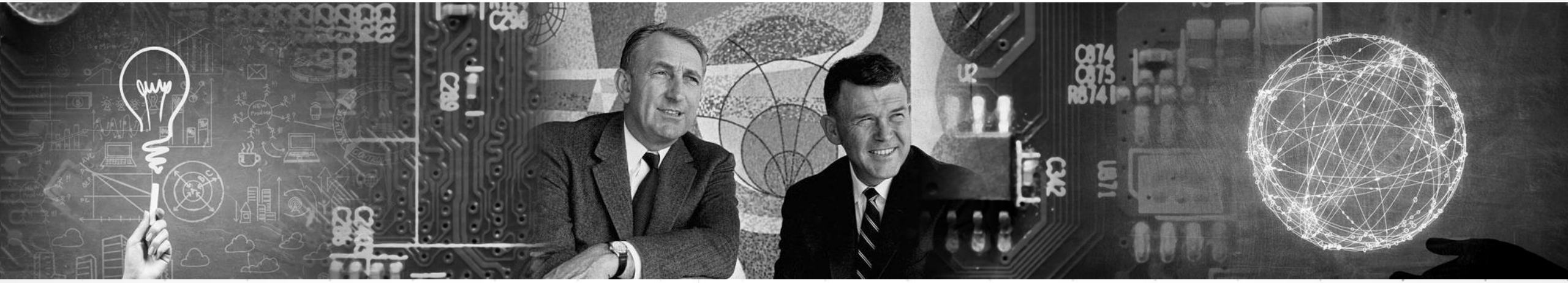
KEYSIGHT TECHNOLOGIES

Keysight Helps You Get to Market Faster

WE HELP YOU CREATE. INNOVATE. AND DELIVER WHAT'S NEXT.



The innovation leader in electronic design and test for over 80 years

Founded in 1939 by Bill Hewlett and Dave Packard as HP with an ongoing mission to help create new markets

Trusted hardware, innovative software and a global network of experts

A Brief History of Keysight

1939–1998: Hewlett-Packard years

A company founded on electronic measurement innovation

1999–2013: Agilent Technologies years

Spun off from HP, Agilent became the World's Premier Measurement Company

In September 2013, it announced the spinoff of its electronic measurement business

2014+: Keysight years

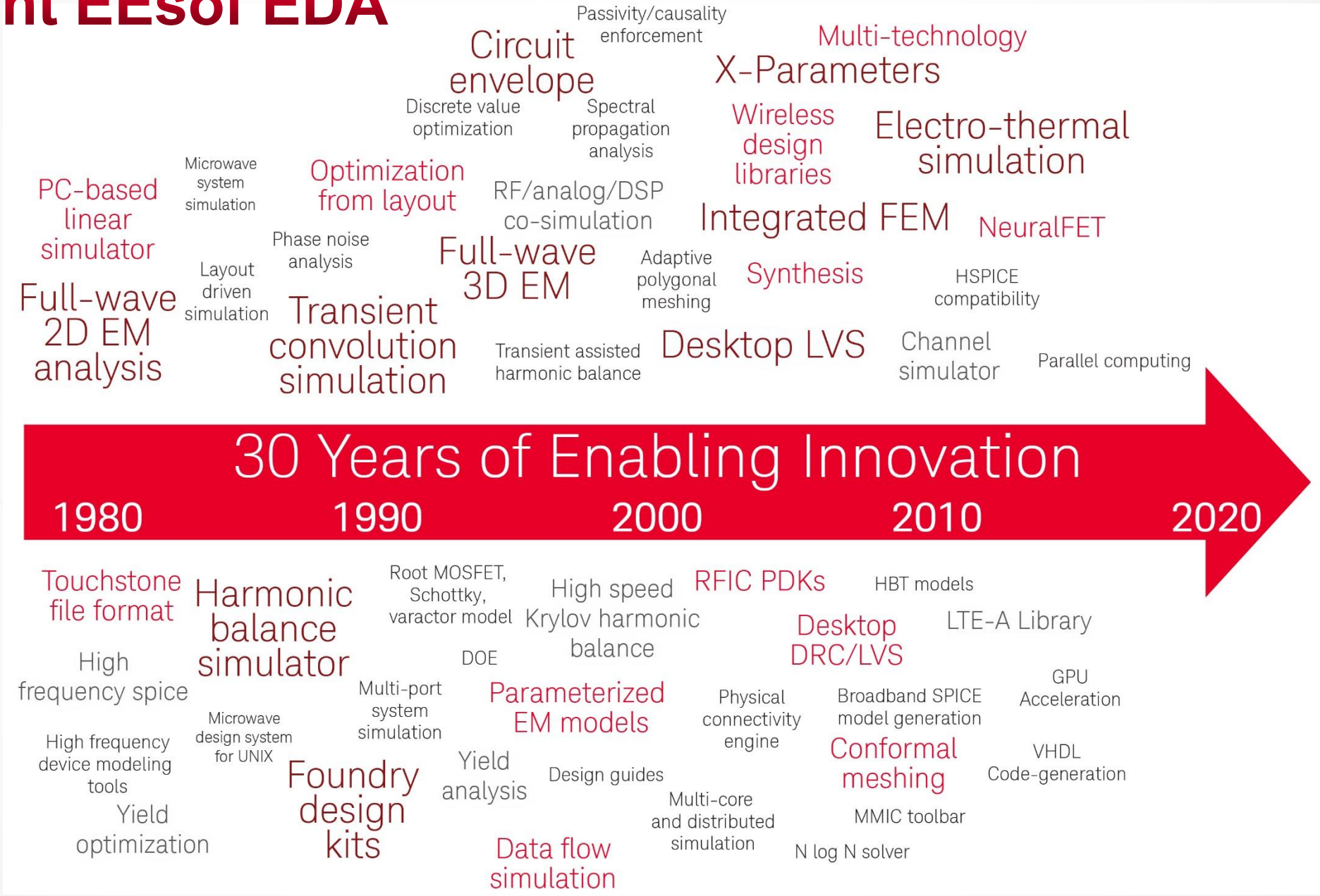
On November 1, Keysight became an independent company focused on the electronic measurement industry

Keysight at a Glance

REVENUE IN FY18	$3.9 billion (~64% from outside U.S)
EMPLOYEES	~12,900
PRESIDENT and CEO	Ron Nersesian
GLOBAL HEADQUARTERS	Santa Rosa, California
CUSTOMER LOCATIONS	100+ countries
MANUFACTURING AND R&D LOCATIONS	U.S., Europe, Asia Pacific
NYSE	KEYS

Ron Nersesian
President and CEO

Keysight EEsof EDA



‘Back in the Day’….Circuit Design with Touchstone Netlist

```
Touchstone/RF (TM) - Configuration( 100 1600 102 30223 3558 1000 1 1196 )
             LOADPUL.CKT    Wed Jan 09 14:39:31 1991

!  CIRCUIT TO AID THE GENERATION OF THEORETICAL LOAD-PULL CONTOURS
!           USING THE TECHNIQUE DEVISED BY S.C.CRIPPS
!NOTE THAT THE IMPEDANCE CALCULATED IS FOR OPTIMUM POWER OUTPUT AND IS THE
!           CONJUGATE OF THE OPTIMUM LOAD IMPEDANCE REQUIRED
!D.J.MORRIS 9/1/91

DIM
  FREQ GHZ
  RES OH
  IND NH
  CAP PF
  ANG DEG

VAR
!  INPUT FET DATA AS FOLLOWS:-
!
 VDSS=10     !DRAIN-SOURCE VOLTAGE AT WHICH Idss IS MEASURED [Volts]
 IDSS=600    !SATURATED DRAIN CURRENT MEASURED WITH Vg=0V [mA]
 CDS=0.600   !DRAIN-SOURCE CAPACITANCE [pF]
 LD=0.300    !DRAIN BOND INDUCTANCE [nH]
 RD=0.00     !DRAIN RESISTANCE [ohms]

EQN
 ROPT=(VDSS)/(0.5*(IDSS/1000))
                            !                  Rd          Ld
CKT                         !
 IND 1  2  L^LD             !   ____________####_____%%%%%__
 RES 2  3  R^RD             !  !          !
 RES 3  0  R^ROPT           !  ---  Cds   [] Ropt          <----!
 CAP 3  0  C^CDS            !  ---        []                    !
 DEF1P 1  TEST              !  !          !                     !
                            !  !__________!___________________  !
OUT                         !                          Conjugate!
 TEST S11                   !                          of required
 TEST RE[Z1]                !        FET Model Elements load impedance
 TEST IM[Z1]                !

FREQ
 SWEEP  4.0 12.0  1.0

GRID
 RANGE  2.0  18.0  2.0
 GR1    -20   0    5
```

Touchstone/RF (TM) - Configuration(100 1600 102 30223 3558 1000 1 1196)
LOADPUL.OUT   Wed Jan 09 14:43:16 1991

FREQ-GHZ	MAG[S11] TEST	ANG[S11] TEST	RE[Z1] TEST	IM[Z1] TEST
4.00000	0.314	-161.635	26.610	-5.836
5.00000	0.360	-163.583	23.899	-5.591
6.00000	0.408	-166.903	21.252	-4.714
7.00000	0.456	-171.122	18.792	-3.336
8.00000	0.502	-175.916	16.578	-1.587
9.00000	0.547	178.939	14.626	0.423
10.0000	0.590	173.602	12.924	2.608
11.0000	0.630	168.186	11.452	4.905
12.0000	0.668	162.774	10.181	7.266

Normalised to 50Ω

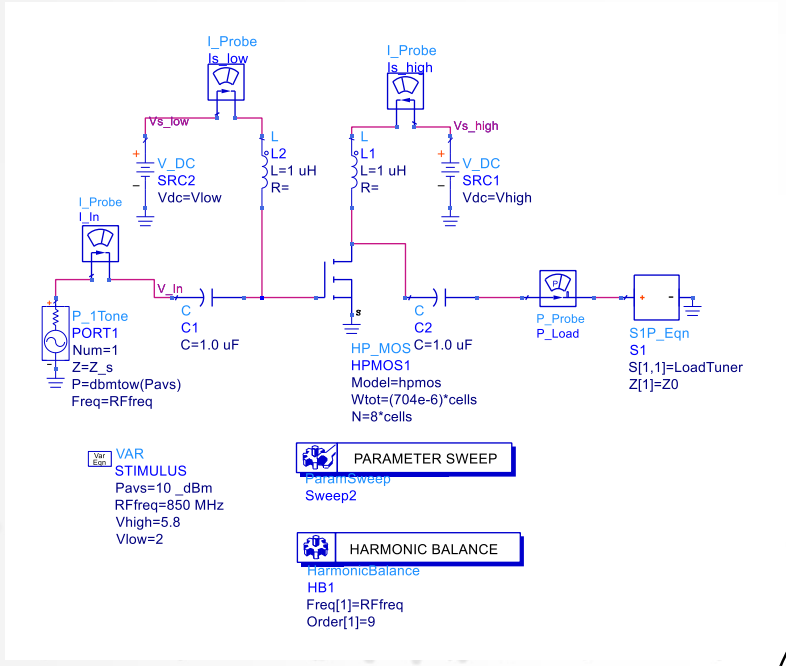
= 0.331

= -0.031

Γ^*_{Lopt} 0.331 − j 0.031

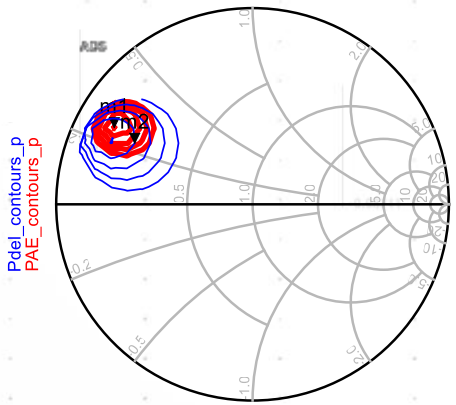
∴ Γ_{Lopt} = 0.331 + j 0.031

‘Today’…. Circuit Simulation in Keysight ADS



System Reference Impedance: 50.000

PAE (thick) and Delivered Power (thin) Contours



Set Delivered Power contour step size (dB) and PAE contour step size (%), and number of contour lines

Eqn Pdel_step=0.5

Eqn PAE_step=2

Eqn NumPAE_lines=5

Eqn NumPdel_lines=5

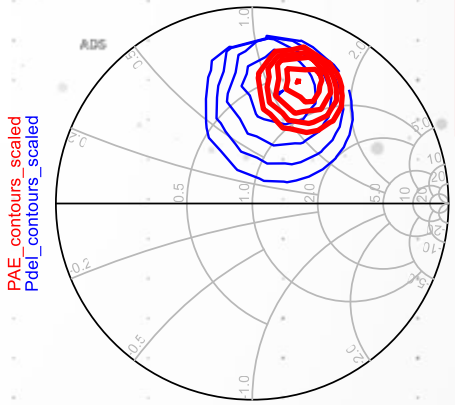
Maximum Power-Added Efficiency, %: 42.32

Maximum Power Delivered, dBm: 25.67

m1
indep(m1)=6
PAE_contours_p=0.805 / 151.007
level=42.217, number=1
impedance = Z0 * (0.115 + j0.255)

m2
indep(m2)=12
Pdel_contours_p=0.676 / 152.580
level=25.162, number=1
impedance = Z0 * (0.204 + j0.234)

Re-Normalized PAE (thick) and Delivered Power (thin) Contours



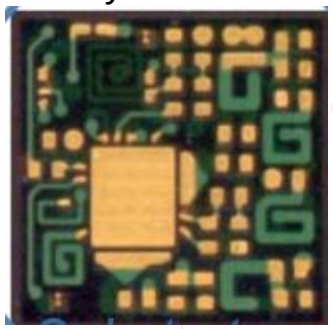
Set new reference impedance:

Eqn Z0new=10

Today…. Beyond Basic Circuit Simulation

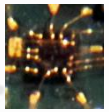
PA IC

Multilayer Substrate



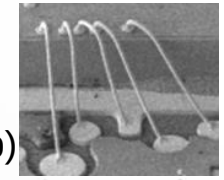
CTRL IC

SWITCH IC

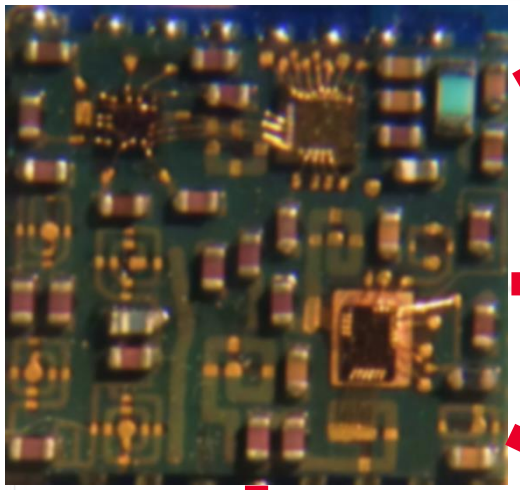


SMTs

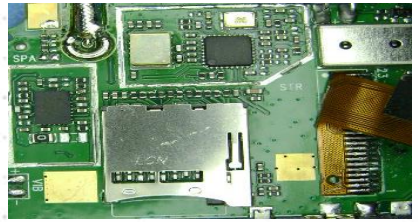
Wirebonds (or ball bump)



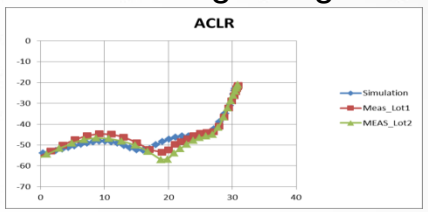
PA / Front End Module



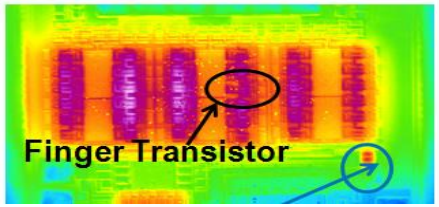
Insensitive to environment



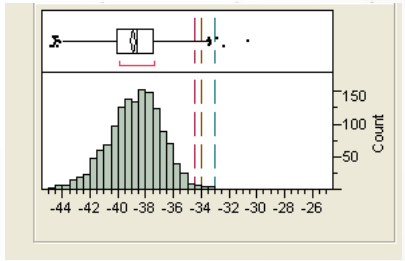
Meets Design Targets



Reliable



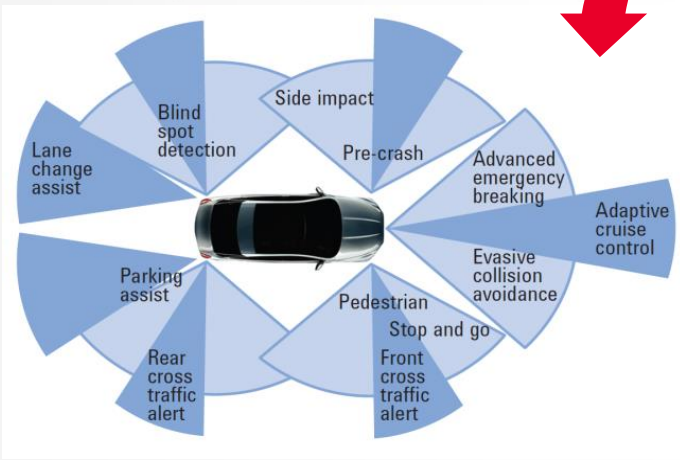
High Yield



Simulation Millimeter-wave Design Eco-System

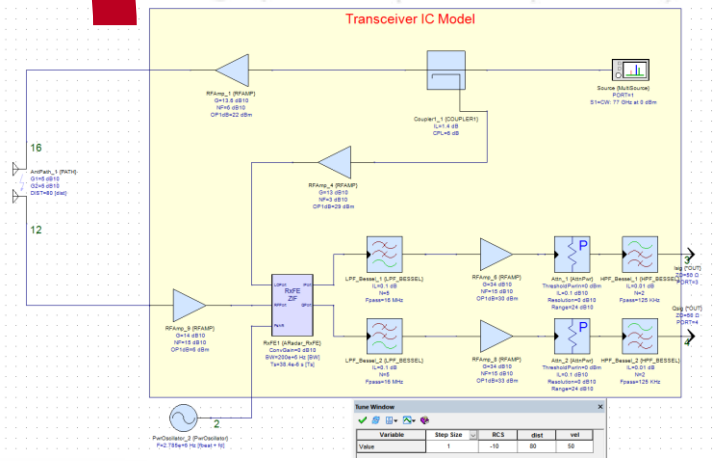
System Level

(eg Complex environment scenario modelling to assess performance metrics such as low speed target detection (micro-doppler))



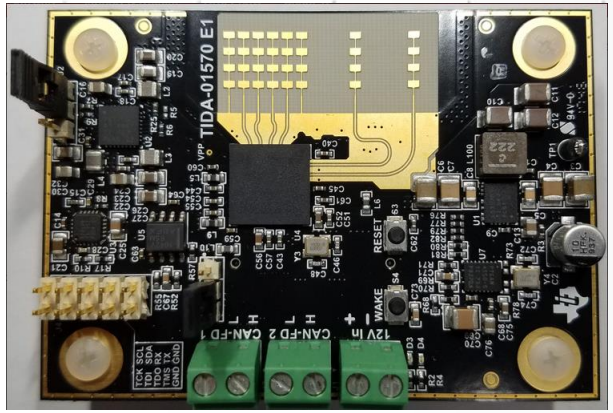
Sub-System Level

(eg Transceiver Simulation to assess performance metrics such as Range, Velocity, RCS)



Circuit Level

(eg LNA Simulation to assess performance metrics such as Gain, Noise Figure, IP3)



Circuit Design Challenges

- PCB : Highly Integrated Circuitry & Antenna array
- RFIC/MMIC Packaging
- IC Design
  - Silicon RFIC
  - Compound Semiconductor MMIC
- Accuracy of Component Models
- Ability to Simulate with Application Specific Stimulus

Typical Circuit Level Design

Generally built using two types of model

- Linear (Analytic, S-parameter (Measured or EM extracted))
- Non-Linear (Compact Models, Measurement Based (X-Parameters etc…))

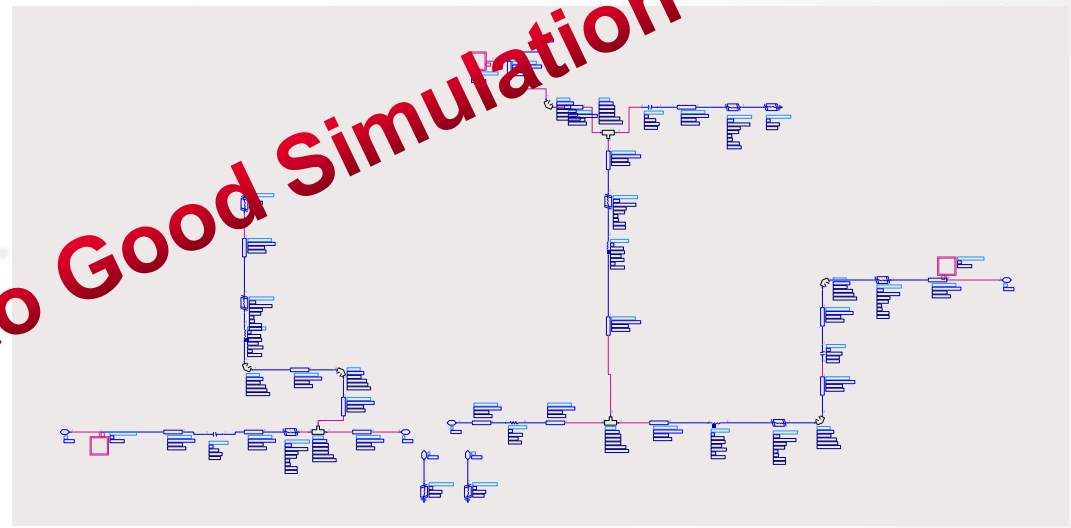
Many ‘Circuit’ Simulation Available

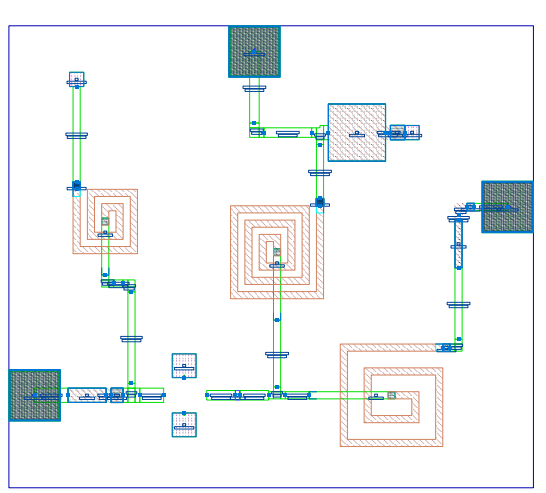
- DC
- AC
- S-parameter
- Harmonic Balance
- Transient
- Circuit Envelope

Extending the analysis beyond just ‘Circuit’ Simulation

- Tuning
- Optimisation
- DFM
- Yield Analysis
- DOE

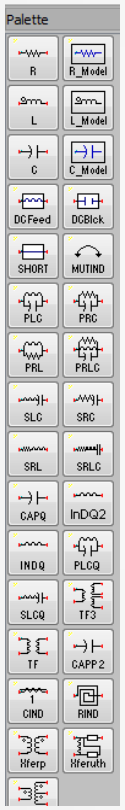
Good Models are Critical to Good Simulation

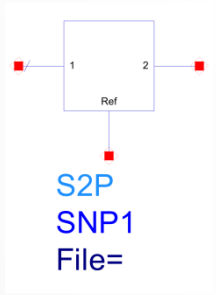




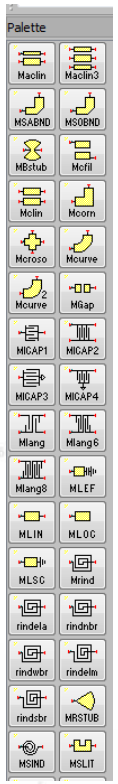
Passive Device Models

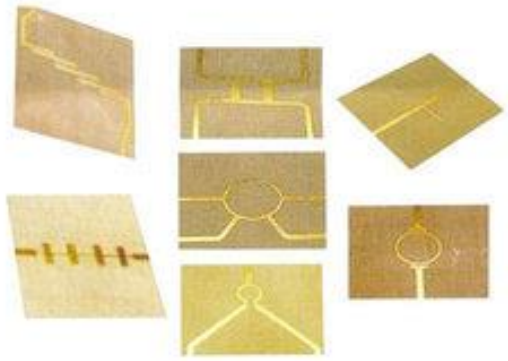
Discrete





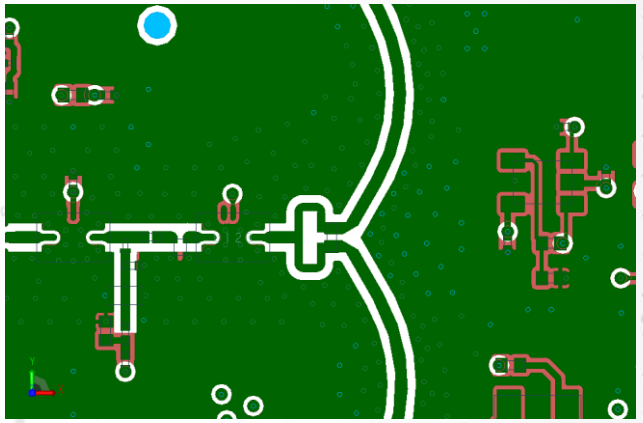
Distributed



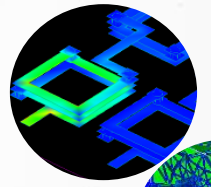


W. J. Getsinger, "Measurement and Modeling of the Apparent Characteristic Impedance of Microstrip," *MTT-31,* August 1983.
E. Hammerstad and O. Jensen, "Accurate Models for Microstrip Computer-aided Design," *MTT Symposium Digest* , 1980.
M. Kirschning and R.H. Jansen, "Accurate Model for Effective Dielectric Constant of Microstrip and Validity up in Millimeter-Wave Frequencies," *Electron* . Lett, Vol. 18 March 18, 1982, pp. 272-273.
M. Kobayashi, "Frequency Dependent Characteristics of Microstrips on Ansiotropic Substrates," *IEEE Trans* ., Vol. MTT-30, November 1983, pp. 89-92.
M. Kobayashi, "A Dispersion Formula Satisfying Recent Requirements in Microstrip CAD," *IEEE Trans* ., Vol. MTT-36, August 1990, pp. 1246-1370.
E. Yamashita, K. Atshi and T. Hirachata, "Microstrip Dispersion in a Wide Frequency Range," *IEEE Trans* ., Vol. MTT-29, June 1981, pp. 610-611.
H. A. Wheeler, "Formulas for the Skin Effect," *Proc. IRE,* Vol. 30, September, 1942, pp. 412-424

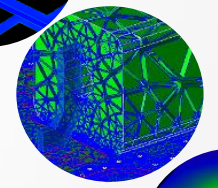
Electromagnetic



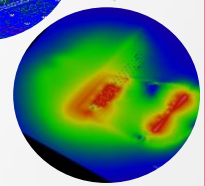
MoM (Method of Moments)
- 3D Planar
- Frequency Domain



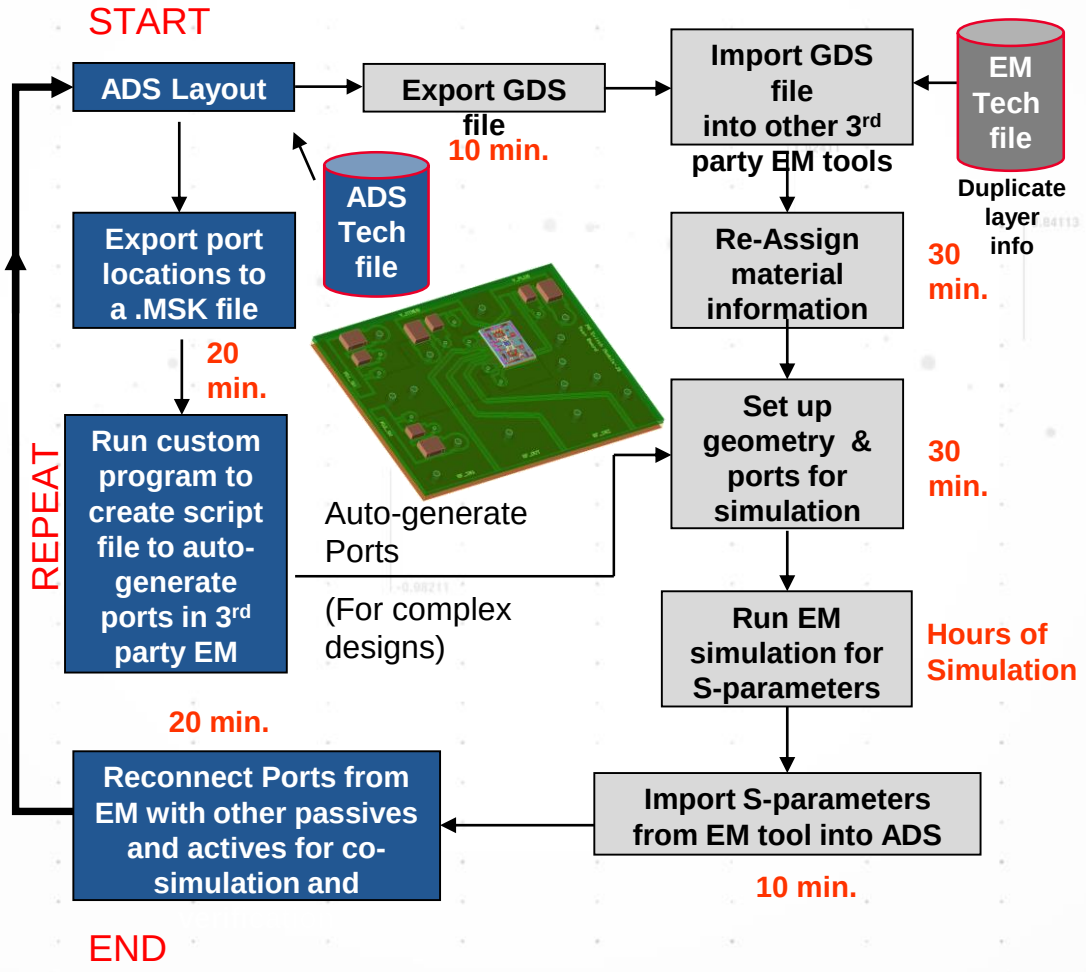
FEM (Finite Element Method)
- Full 3D
- Frequency Domain



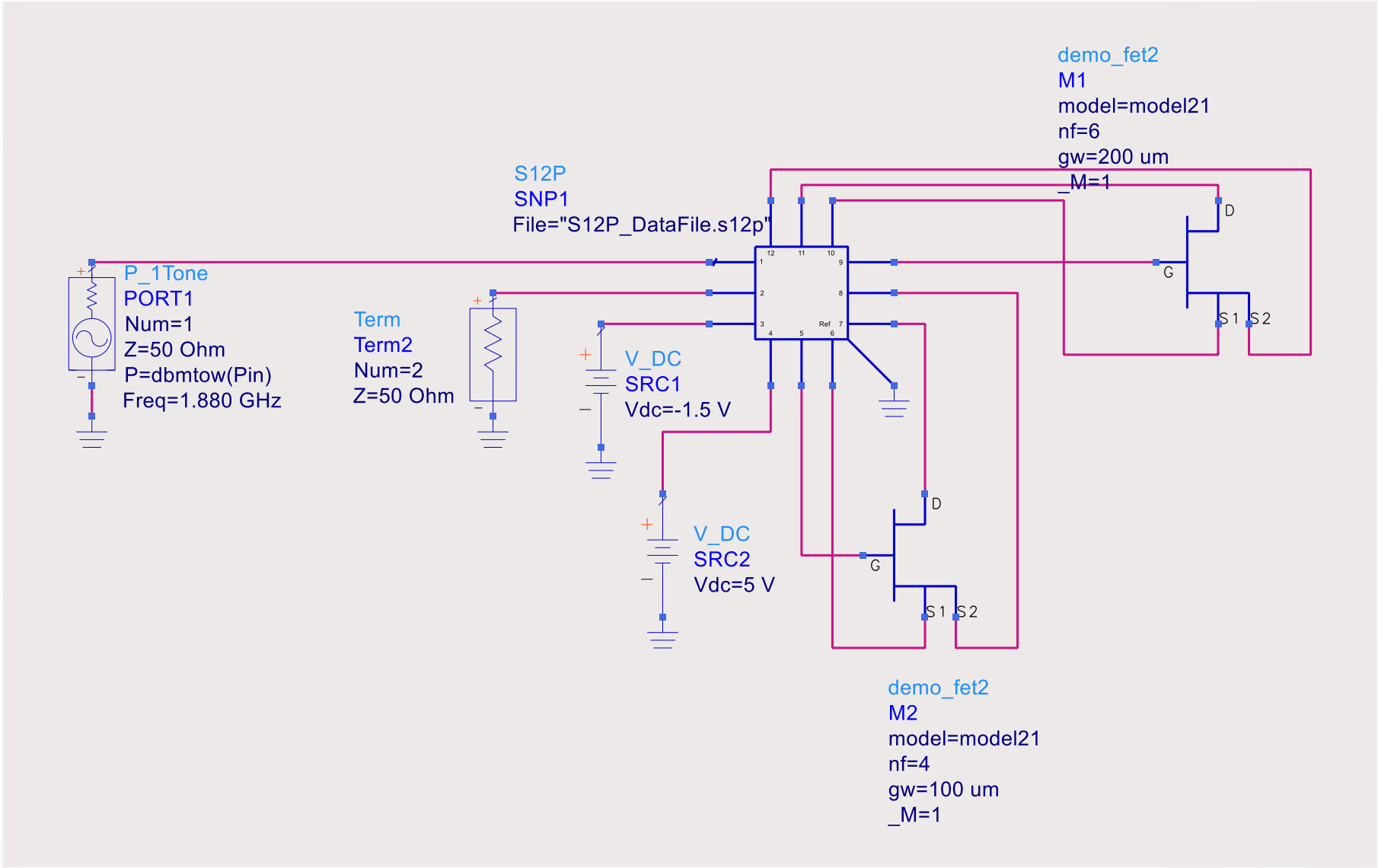
FDTD (Finite Difference Time Domain)
- Full 3D
- Time Domain



Traditionally EM simulation has been performed in stand-alone 'Guru' tools – Disconnected form the Circuit Design Flow



Traditional Design Flow : EM simulation in Circuit Flow



A Better Way with RFPro: EM for every RF circuit designer

GIVE UP COMPLEXITY

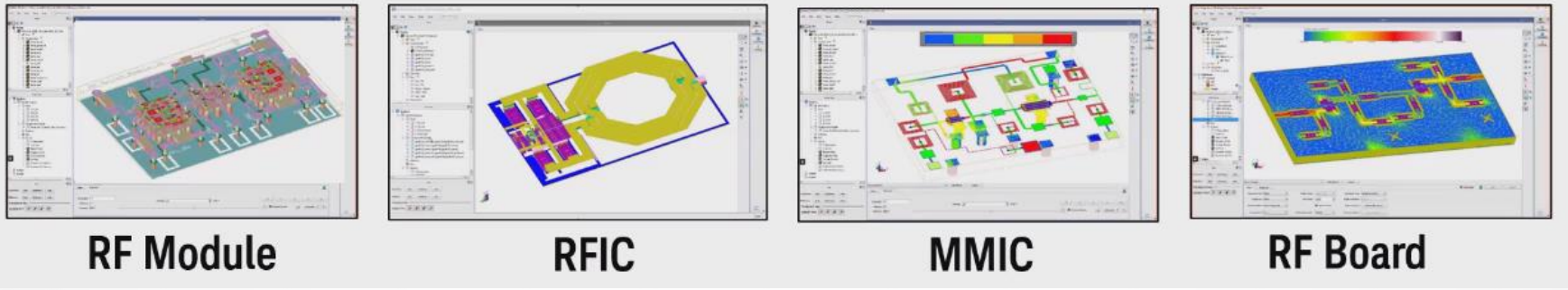
- Main customer requests for the EM flow

- Layout
  - ✓ No Cookie cutting
  - ✓ No exporting
  - ✓ No manual removing active devices and placing pins & ports
  - ✓ No manual reconnecting schematics to s-parameter files

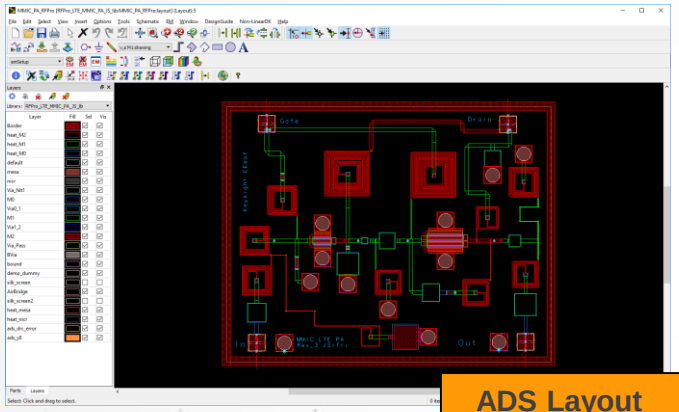
- Solver
  - ✓ No expert setup
  - ✓ Be confident in the setup of the simulation and accuracy of the results
  - ✓ Better automated defeaturing (via merging/dummy removal/hatched planes…)

- Integration
  - ✓ 3D view
  - ✓ Solution for RF PCB, RFIC, MMIC and RF Modules
  - ✓ Same user interface for ADS and Cadence Virtuoso
  - ✓ Same environment for FEM and Momentum

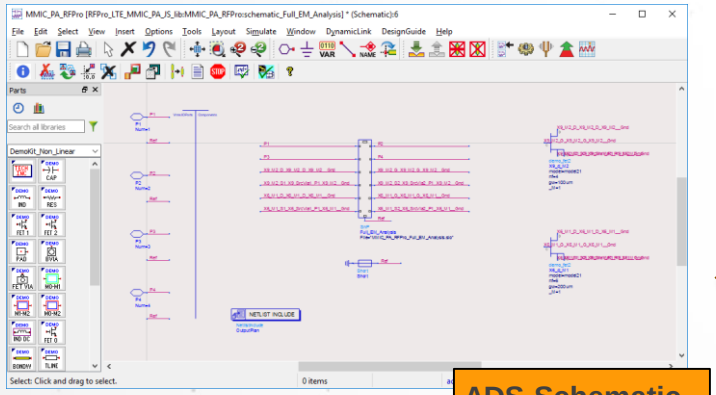
RFPro



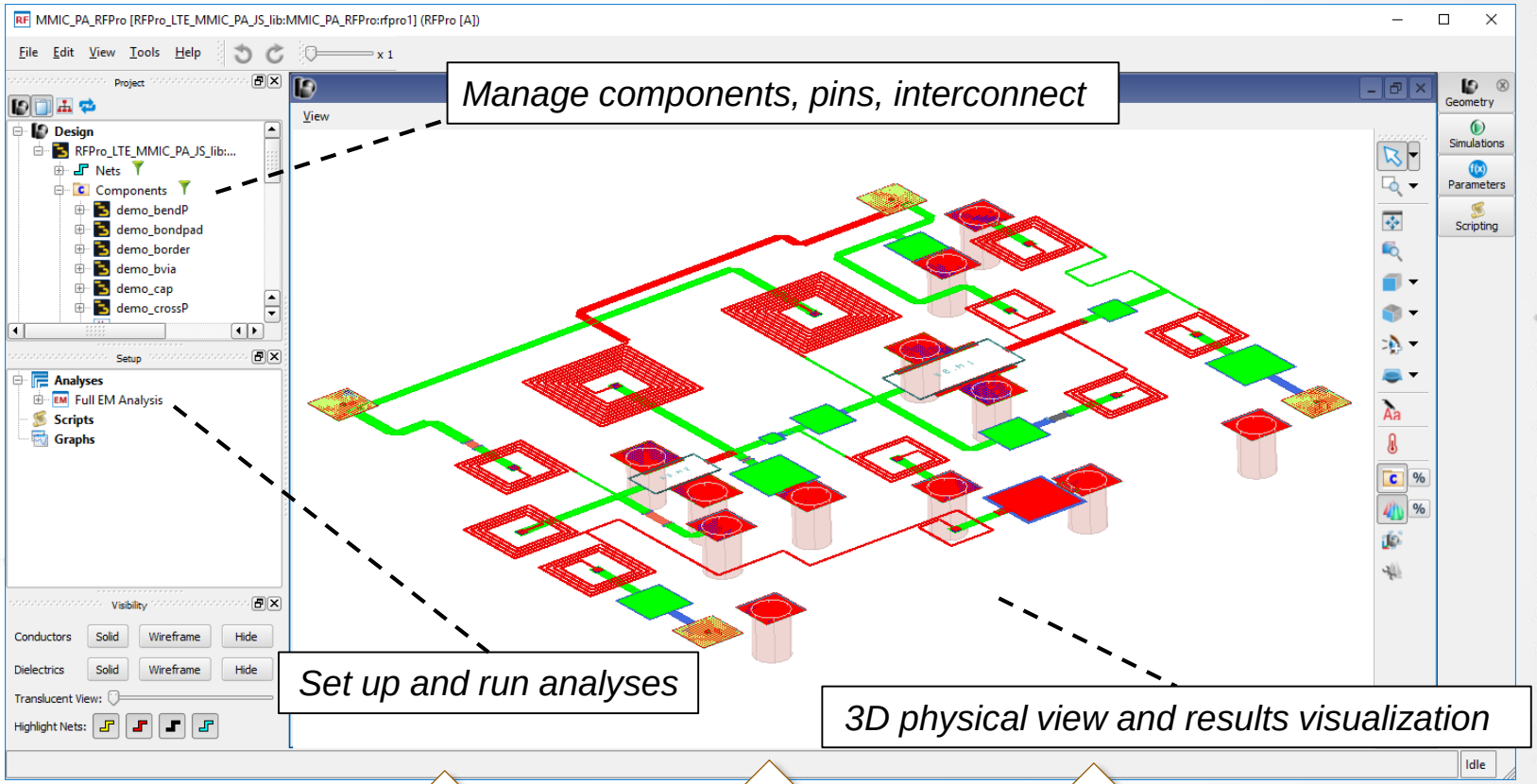
New Design Flow : EM simulation in Circuit Flow with RFPro



ADS Layout



ADS Schematic



Manage components, pins, interconnect

Set up and run analyses

3D physical view and results visualization

Momentum RF

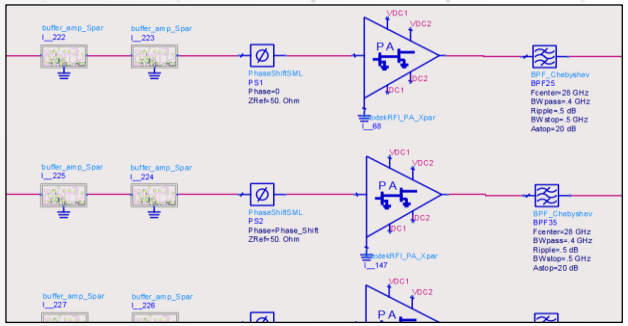
Momentum uW

FEM

Advanced Capabilities: EM with Circuit Excitation

HB, S-Par, Envelope, Tran, DC, AC

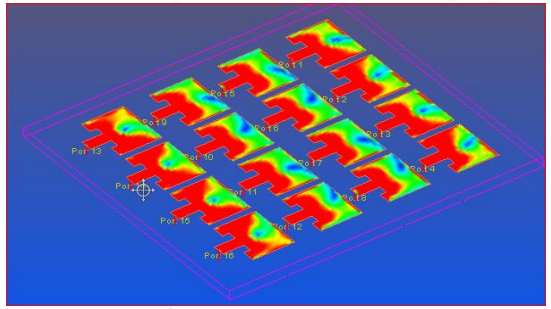
Transceiver Components



Circuit level designs; X-parameter models, EM models, etc.

+

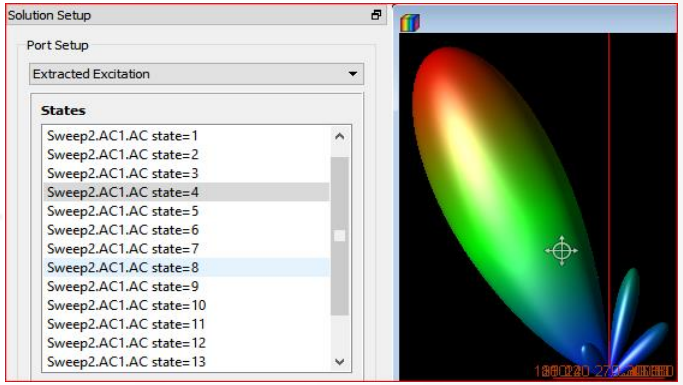
Antenna and other physical structures



Momentum Planar EM
Full 3D FEM Simulation

=

Complete EM / Circuit Simulation and Analysis

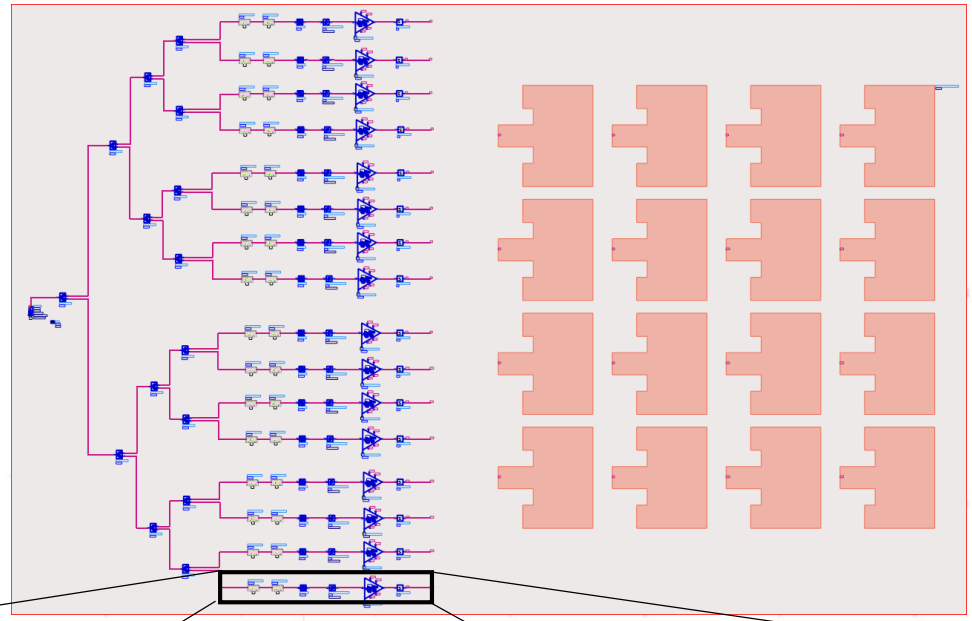


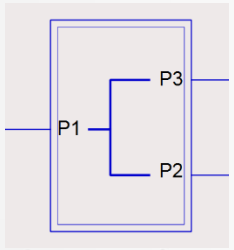
Captures the excitation from the T/R module and apply it to the Antenna(s)

The output from the circuit simulation drives/excites the Antenna ports

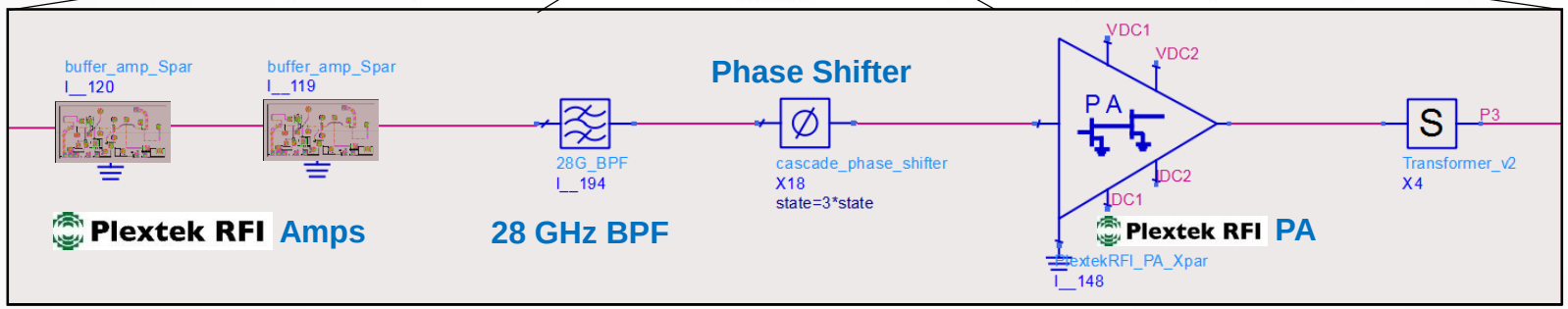
28 GHz Transmit Chain with Patch Antenna

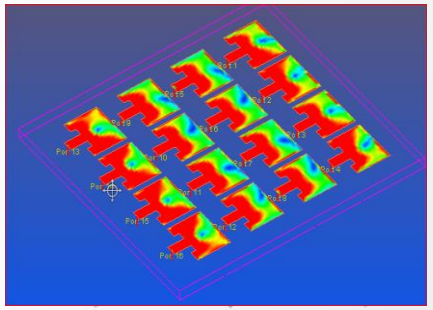
System / Circuit / EM Co-simulation and beam steering





Power Divider

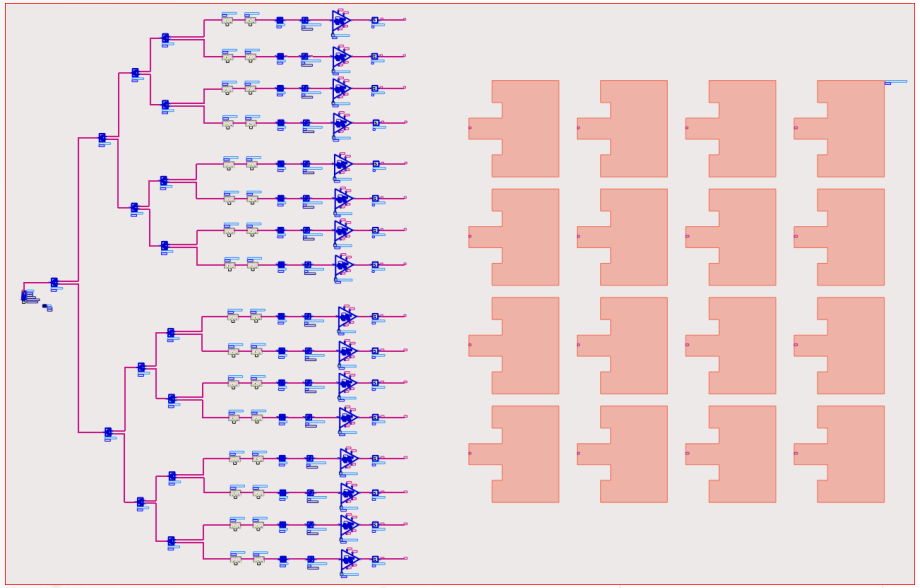


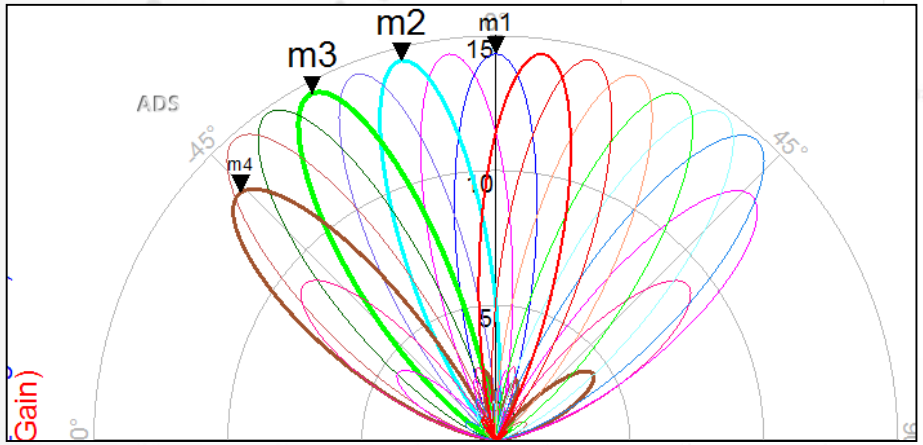


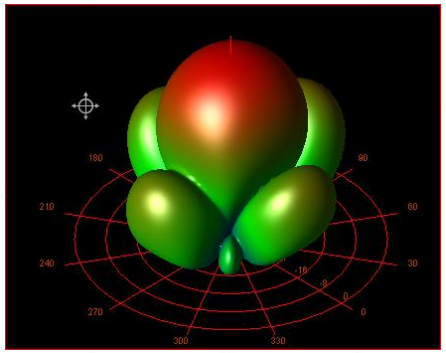
4X4 Array .5 Lambda Patch Antenna

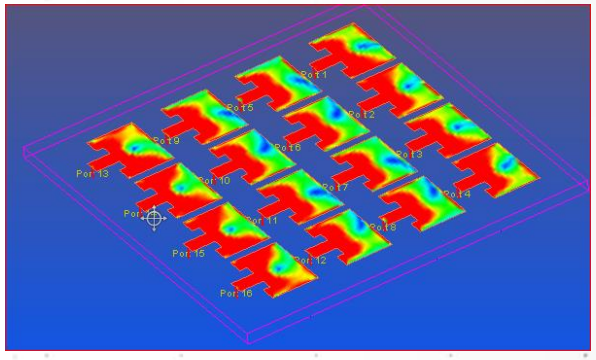
28 GHz Transmit Chain with Patch Antenna

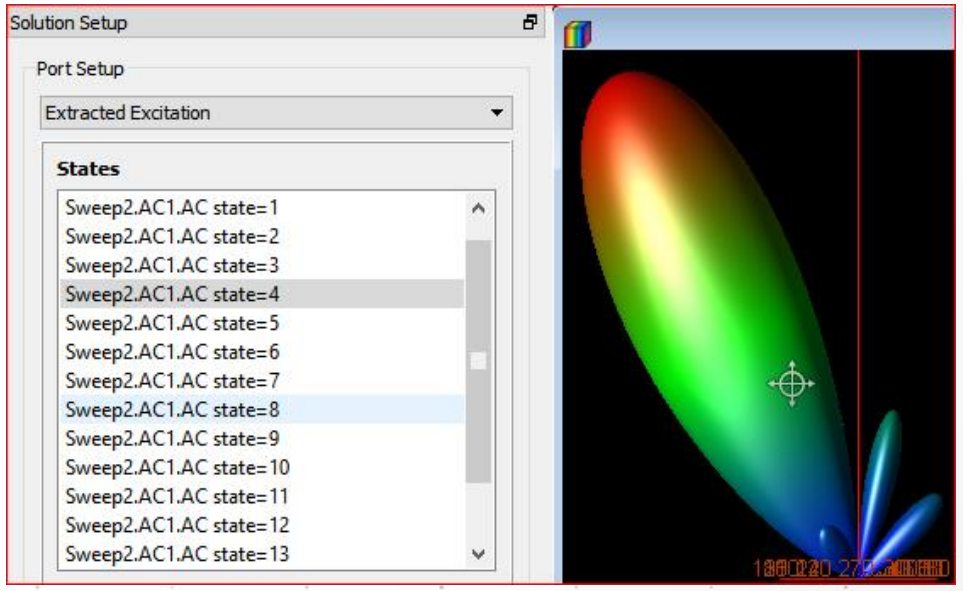
System / Circuit / EM Co-simulation and beam steering



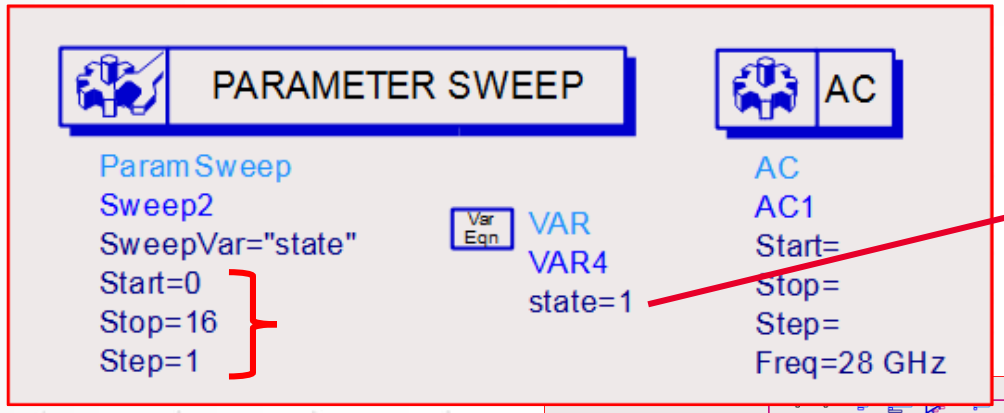






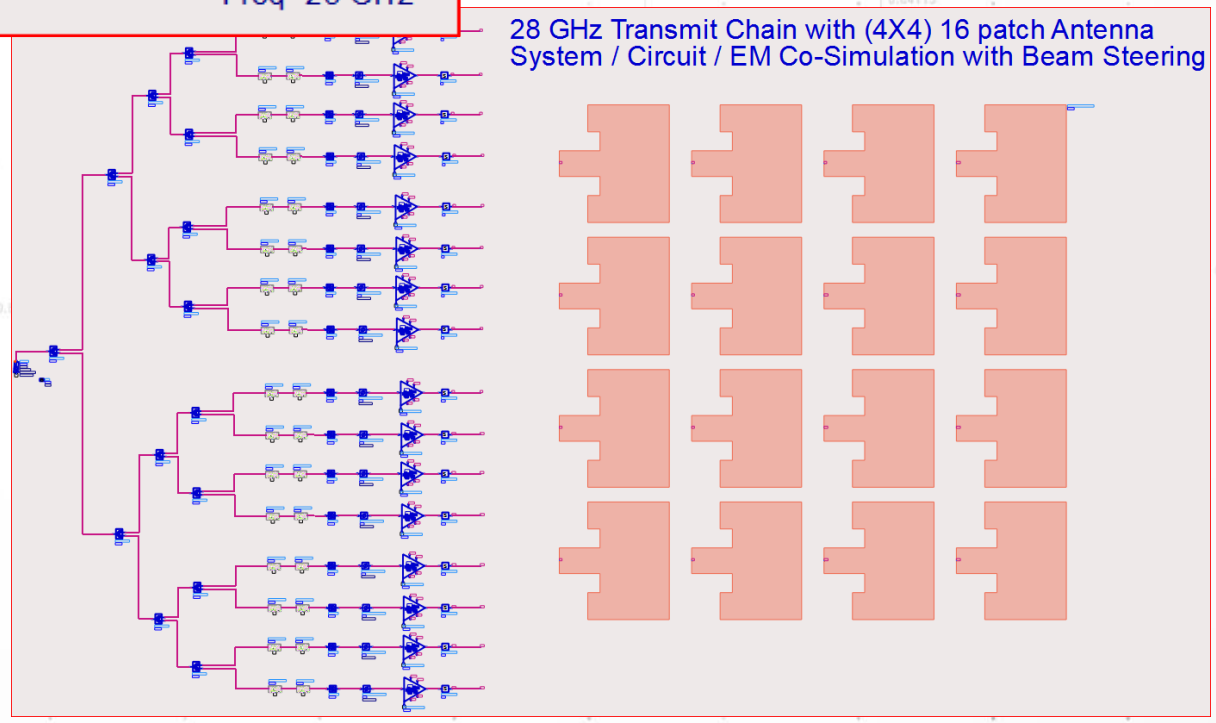


Sweeping the Phase Shifter for Different Look-up Angles



Phase Shift	Antenna look-up angle
61.5 degrees	20 degrees
31.2	10
22.5	7.2

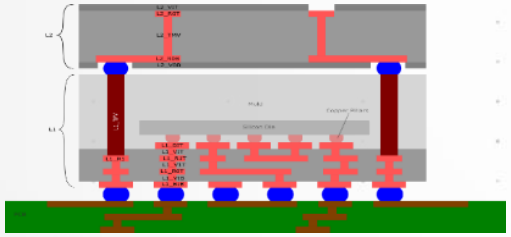
There is a mathematical relationship between the Phase-shifter phase angle and the Antenna beam look-up angle



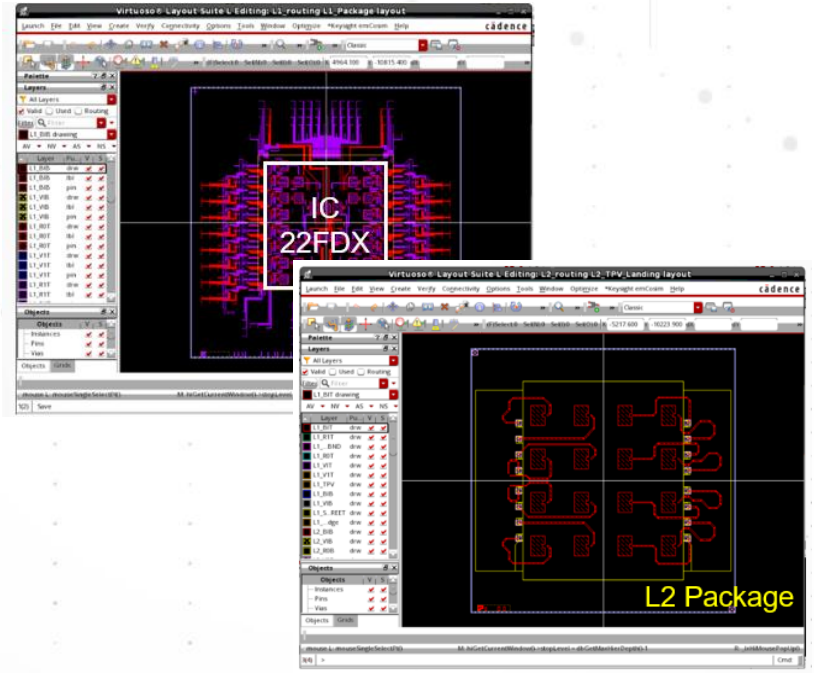
Success Story: Packaging at mmW frequencies

REGION:EMEAI, GERMANY

- **Company Name**
  - GlobalFoundries (Germany)
  - Fraunhofer IIS (Germany)
- **Device**
  - mmW transceiver with antenna in package
- **Customer Challenge**:
  - Find a flow to be able to assess impairments between the IC and the antennas

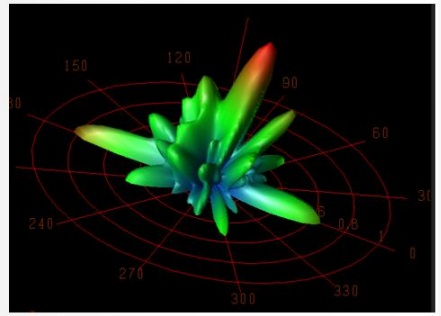


- **Solution:**
  - Using ADS and emCosim to assemble the package and simulate the impairments



- **Products Used in Solution:**
  - ADS, FEM

- **Results**:
  - Good correlation between results and expectations



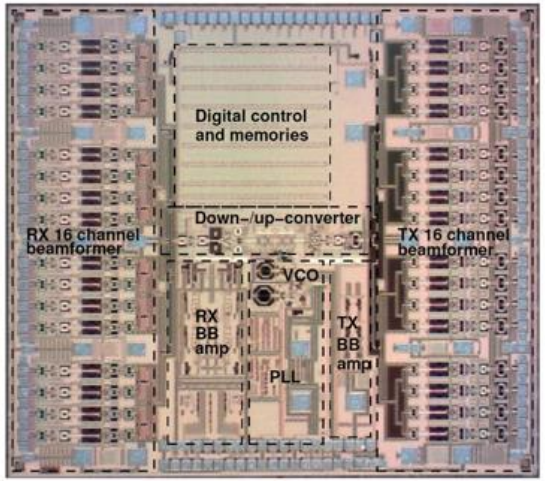
Success Story: Modulated signals (WLAN 802.11ad)

REGION:EMEAI, SWEDEN

SIVERSIMA

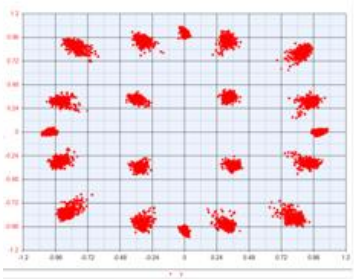
- **Company Name**
  - Sivers IMA (Stockholm, Sweden)
- **Device**
  - WLAN802.11ad transceiver
- **Customer Challenge**:
  - Shorten design cycle by 1spin by optimizing LoadPull on EVM

- **Solution:**
  - Using custom VTBs inside Cadence Virtuoso with GG

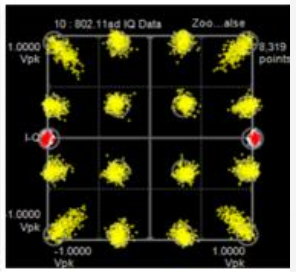


- **Products Used in Solution:**
  - SystemVue, Momentum, GoldenGate

- **Results**:
  - Extremely good correlation between results and measurements and **1 spin saved**
  - 3 dB gained on the RF chain vs old methodology



VTB simulated TX constellation with GoldenGate



Measured TX constellation with WWC/VSA

Supporting Materials

UPCOMING WEBINARS / RECORDED WEBINARS

Designing an Award-Winning mmWave RFIC: Experiences and Insights
Wednesday, May 15, 2019, 11:00 AM CEST

Design and Simulation of 5G 28-GHz Phased Array Transceiver
Original broadcast August 3, 2017

mmWave Antenna Design Made Easy in ADS
Original broadcast February 2, 2017

Designing Phased Arrays With Confidence
Original broadcast May 3, 2018

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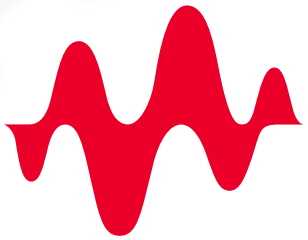

KEYSIGHT
TECHNOLOGIES